

A5

a bus bridge, comprising a bus interface, operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive the selected signal via a third internal signal path; and

an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

REMARKS

Applicants respectfully traverse and request reconsideration.

Claim 21 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim Applicants' subject matter due to a typographical error with reference to "the internal circuit". Applicants have corrected the typographical error.

Claims 1-39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,141,021 (Bickford et al.). The Bickford reference is directed to a method and apparatus for eliminating contention on an accelerated graphics port (AGP) wherein a motherboard includes an AGP graphics accelerator chip and has a connector coupled to an accelerated graphics port that is adapted to receive an AGP graphics accelerator add-in card. A disable device 124 prevents a FRAME # signal driven by a PCI bus master to indicate the start of a configuration transaction, is prevented from reaching the AGP graphics accelerator that is to be disabled. (Col. 5, lines 1-5). The disabling device may be a metal jumper or a passthrough circuit such as that shown in FIG. 6. In all cases, Bickford teaches to disable a graphics accelerator during configuration by routing the FRAME # signal from the PCI to the desired graphics accelerator. Since the other graphics accelerator does not receive the FRAME # signal, the other graphics accelerator is not enabled. In all cases as described by Bickford, the disable device is coupled to the PCI bus to route the FRAME # signal to a selected AGP graphics accelerator. The Bickford reference is silent as to addressing echoes or signal reflections from expansion slots for an external graphics controller card and in fact, teaches away from addressing

the problem since all embodiments appear to be shown with the AGP bus 110 being coupled directly to the AGP add-in card connector or to the AGP controller. In fact, the Bickford reference teaches using a completely different approach from that claimed by Applicants. The Bickford reference suffers from the same problems described in Applicants' "Background of the Invention" section since the expansion slot AGP bus lines of Bickford are not isolated, but instead are coupled as with conventional configurations.

In contrast, Applicants' invention addresses the problem of echoes or signal reflections from an expansion slot that can interfere with on chip graphics controllers' reception of signals.

As to claim 1, for example, Applicants claim a first internal circuit, such as an internal bus bridge or internal graphics processor, that provides a first internal signal via an internal signal path. An input buffer is operable to receive a first external signal, such as from an external graphics processor, via a external signal path. A selector circuit is coupled to both the first internal circuit and to the input buffer. The selector circuit is coupled to the first internal circuit via the internal signal path and is operable to select either the first internal signal or the external signal to provide as a selected signal. As such, among other advantages, the input buffer isolates the external signal path from the first internal circuit. No such input buffer isolation or selector circuit is taught or suggested by the cited reference. In fact, the disable device 124 of Bickford does not select internal signals or external signals as alleged in the Office Action. To the contrary, the disable device 124 merely regulates whether an internal FRAME # signal is passed to an external or internal AGP graphics processor as shown and described, for example, with respect to FIG. 6.

In addition, the Office Action admits that Bickford does not disclose the claimed input buffer and hence the corresponding structure with respect to the selector circuit and first internal circuit. The Office Action takes official notice that it is common practice to allegedly use an input buffer with the AGP as claimed. Applicants respectfully note that Bickford teaches away from using Applicants' claimed input buffer by showing that there is no isolation between the AGP bus and the expansion slot or onboard AGP graphics adaptor. In fact, Bickford uses a completely different approach.

Moreover, if one were to add an input buffer to Bickford, Applicants respectfully submit that there would be no difference in operation from the Bickford device since Bickford teaches to control the FRAME # signal going to the graphics accelerators without isolating any reflection paths from, for example, the external signals. As such, even combining an internal buffer as alleged in the Office Action with Bickford, would still fail to teach Applicants' claimed invention.

Applicants also respectfully submit that there is no motivation other than Applicants' own specification, to combine an input buffer as claimed to an external signal path and selector as claimed. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

As to claim 21, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and again note that this claim requires, among other things, a bus bridge signal from an internal bus bridge and receiving, by an internal circuit, the bus bridge signal and further that an internal I/O circuit prevent signals from any external circuit from reaching the internal circuit. Again, as noted above, Bickford does not teach or suggest an internal I/O circuit that prevents signals from an external circuit from reaching an internal circuit, but in fact allows all external signals to pass to the AGP bus connected to the internal circuit. Accordingly, this claim is also believed to be in condition for allowance.

As to claim 29, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and again note that Bickford does not teach an integrated bus bridge graphics unit coupled to memory that includes an internal circuit operably configured to void signals from an external graphics bus. Since Bickford teaches that the internal graphics bus is coupled directly to the external slot and to the internal AGP graphics chip (See FIG. 3), no isolation of a bus is provided by Bickford. Bickford simply controls the receipt of a FRAME # signal from the PCI bus to either of the two graphics controllers to enable one of the two graphics controllers to operate. As such, this claim is also believed to be in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter and are also allowable. For example, as to claim 2, it is alleged that the Bickford reference discloses an output buffer (structure 170) and provides a second internal signal via the first external signal

path. The Office Action admits that Bickford does not disclose, among other things, a separate second internal signal path for conveying signal to the output buffer. The Office Action, however, alleges that duplication of working parts of the device which are normally formed in two pieces is well known and that routine skill in the computer art would only be needed to add an additional internal signal path and to integrate the external output path and external input path into one external path. Applicants respectfully note that amended claim 2 indicates for clarification that the output buffer is operative to receive the first internal signal via the second internal path and to provide the second internal signal via the first external signal path. Such a combination of internal circuit, input buffer, output buffer and selector circuit is not taught or suggested by the cited references.

As to claim 16, Applicants note that this claim differs from that of 2 and 17 but that the Office Action does not address the claim limitations of this claim. Applicants respectfully note that this claim requires, among other things, a bus bridge, that includes a bus interface that provides a second internal signal to the first internal circuit and an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal by the first external signal path such that the input buffer and selector circuit are inoperable to receive the second internal signal. Then Bickford does not teach or suggest the bus bridge in combination with the output and input buffer as claimed. Accordingly, this claim is also believed to be in condition for allowance.

As to claim 20, the claim requires, among other things, that the input buffer is inoperable to provide the external signal from the first external signal path to the first internal circuit and that the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit. This isolation is not taught or suggested by Bickford and as such, this claim is also believed to be in condition for allowance.

New claim 40 is allowable, at least for the same reasons as claim 1, and in addition, the combination of bus bridge, input/output buffer and selector circuit is not taught or suggested by the cited reference. In addition, as noted above, the Bickford disable device 124 does not select one of a first internal signal or an external signal to provide the selected signal, but to the

contrary, merely selects which of two graphics processors receive a FRAME # signal. As such, no isolation is taught or suggested by the cited reference.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Accordingly, Applicant respectfully submits that the Claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By: C. Reckamp
Christopher J. Reckamp
Registration No. 34,414

Date: Jan 23, 2003
VEDDER, PRICE, KAUFMAN &
KAMMHLZ
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please replace the paragraph on page 10, beginning at line 20, with the following rewritten paragraph:

A southbridge 170 couples a PCI bus 160 to an ISA bus 180. [.] The southbridge 170 is a well-known secondary bus bridge, often found in computer systems between buses other than the processor bus, and may be replaced with any other device commonly found on a bus that is coupled to the bus bridge 120.

Please replace the paragraph on page 12, beginning at line 29, and continuing on page 13, ending with line 7, with the following rewritten paragraph:

The internal bus bridge enable flip-flop 106 provides an internal bus bridge enable signal 162 to the internal I/O circuit [118] 140 that allows the bus bridge 120 to issue a second internal signal via a second internal signal path (a first portion of the bufferless data path 122) and an output buffer 164 over the AGP bus extension 192. The internal bus bridge data-out flip-flop 102 aligns the data to comply with the AGP bus protocol, if necessary, within the bus bridge 120 pending issue of the data over the AGP bus 190 (shown in FIG. 4). The signal at the data input of the output buffer 164 is shown connected to the data input of the internal circuit data in flip flop 110, and is driven from the internal bus bridge data out flip flop 102. Any arrangement that affords the bus bridge 120 being able to send a signal to the input of the output buffer 164, and a logically similar signal to the input of the internal circuit data in flip flop 110, applies.

IN THE CLAIMS:

Please amend Claim 2, Claim 21 and add new Claim 40 to read as follows:

2. (Amended) The configurable interface circuit of Claim 1, further comprising: an output buffer operative to receive [a second] the first internal signal via a second internal signal path and to provide the second internal signal via the first external signal path.

21. (Amended) A method for configuring a bus interface circuit comprising: at [the] an internal circuit, receiving a bus bridge signal from an internal bus bridge; and at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit.

40. (New) A configurable interface circuit comprising:
an internal graphics controller operable to provide a first internal signal via a first internal signal path;
an input buffer operable to receive a first external signal via an first external signal path;
a selector circuit coupled to the internal graphics controller via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal;
a bus bridge, comprising a bus interface, operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive the selected signal via a third internal signal path; and
an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.